

Substitution for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Complete if Known

Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

Sheet 1 of 8

Attorney Docket No: 1303.034US1

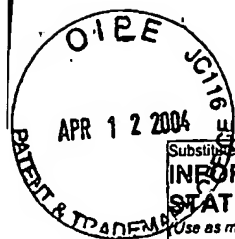
US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
JTR	US20020001965	01/03/2002	Forbes, Leonard	438	734	07/22/1997
JTR	US20020070421	06/13/2002	Ashburn, Stanton P.	257	510	02/08/2002
JTR	US20020185686	12/12/2002	Christiansen, Silke H., et al.	257	347	04/03/2002
JTR	US20030227072	12/11/2003	Forbes, Leonard	257	616	06/10/2002
JTR	US20030027406	02/06/2003	Malone, Farris D.	438	471	08/01/2001
JTR	US20030201468	10/30/2003	Christiansen, H., et al.	257	200	04/30/2003
JTR	US20030218189	11/27/2003	Christiansen, Silke H., et al.	257	200	11/19/2002
JTR	US-4,241,359	12/23/1980	Izumi, Katsutoshi, et al.	257	386	03/02/1978
JTR	US-4,589,928	05/20/1986	Dalton, John V.	438	142	08/21/1984
JTR	US-4,717,681	01/05/1988	Curran, Patrick A.	438	314	05/19/1986
JTR	US-5,426,061	06/20/1995	Sopori, Bhushan L.	438	475	09/06/1994
JTR	US-5,443,661	08/22/1995	Oguro, Shizuo, et al.	148	33.5	07/27/1994
JTR	US-5,461,243	10/24/1995	Ek, Bruce A., et al.	257	190	10/29/1993
JTR	US-5,646,053	07/08/1997	Schepis, Dominic J.	438	402	12/20/1995
JTR	US-5,661,044	08/26/1997	Holland, Orin W., et al.	438	766	06/15/1995
JTR	US-5,691,230	11/25/1997	Forbes, Leonard	437	62	09/04/1996
JTR	US-5,759,898	06/02/1998	Ek, Bruce, et al.	438	291	12/19/1996
JTR	US-5,773,152	06/30/1998	Okonogi, Kensuke	428	446	10/13/1995
JTR	US-5,789,859	08/04/1998	Watkins, Charles M., et al.	313	495	11/25/1996
JTR	US-5,840,590	11/24/1998	Myers Jr., Samuel M., et al.	438	471	12/01/1993
JTR	US-5,879,996	03/09/1999	Forbes, Leonard	438	289	09/18/1996
JTR	US-5,963,817	10/05/1999	Chu, Jack O., et al.	438	410	10/16/1997
JTR	US-5,997,378	12/07/1999	Dynka, Danny, et al.	445	25	07/29/1998
JTR	US-6,001,711	12/14/1999	Hashimoto, Takasuke	438	473	03/09/1998
JTR	US-6,022,793	02/08/2000	Wijaranakula, Witawat, et al.	438	473	10/21/1997
JTR	US-6,054,808	04/25/2000	Watkins, Charles M., et al.	313	495	01/26/1999
JTR	US-6,083,324	07/04/2000	Henley, Francois J., et al.	148	33.2	02/19/1998
JTR	US-6,093,623	07/25/2000	Forbes, Leonard	438	455	08/04/1998
JTR	US-6,093,624	07/25/2000	Letavic, Theodore J., et al.	438	462	12/23/1997

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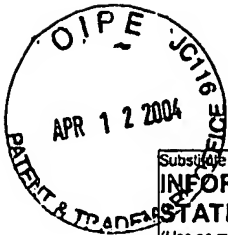
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Attorney Docket No: 1303.034US1

JTR	US-6,127,777	10/03/2000	Watkins, Charles M., et al.	313	554	07/31/1998
JTR	US-6,172,456	01/09/2001	Cathey, David A., et al.	313	495	04/05/1999
JTR	US-6,174,784	01/16/2001	Forbes, Leonard	438	405	11/14/1997
JTR	US-6,204,145	03/20/2001	Noble, Wendell P.	438	412	08/07/1998
JTR	US-6,228,694	05/08/2001	Doyle, Brian S., et al.	438	199	06/28/1999
JTR	US-6,251,751	06/26/2001	Chu, Jack O., et al.	438	439	04/13/1999
JTR	US-6,274,460	08/14/2001	Delgado, Jose A., et al.	438	476	06/17/1999
JTR	US-6,309,950	10/30/2001	Forbes, Leonard	438	455	03/23/2000
JTR	US-6,315,826	11/13/2001	Muramatsu, Satoru	117	95	06/22/2000
JTR	US-6,338,805	01/15/2002	Anderson, Gary L.	216	89	07/14/1999
JTR	US-6,339,011	01/15/2002	Gonzalez, Fernando , et al.	438	473	03/05/2001
JTR	US-6,368,938	04/09/2002	Usenko, Alexander Y.	438	407	06/07/2000
JTR	US-6,376,336	04/23/2002	Buynoski, Matthew S.	438	476	02/01/2001
JTR	US-6,377,070	04/23/2002	Forbes, Leonard	326	41	02/09/2001
JTR	US-6,391,738	05/21/2002	Moore, John T.	438	402	12/20/2000
JTR	US-6,423,613	07/23/2002	Geusic, Joseph	438	455	11/10/1998
JTR	US-6,424,001	07/23/2002	Forbes, Leonard , et al.	257	315	02/09/2001
JTR	US-6,444,534	09/03/2002	Maszara, Witold P.	438	311	01/30/2001
JTR	US-6,448,601	09/10/2002	Forbes, Leonard , et al.	257	302	02/09/2001
JTR	US-6,478,883	11/12/2002	Tamatsuka, Masaro , et al.	148	33.2	04/18/2000
JTR	US-6,496,034	12/17/2002	Forbes, Leonard , et al.	326	041	02/09/2001
JTR	US-6,531,727	03/11/2003	Forbes, Leonard , et al.	257	302	02/09/2001
JTR	US-6,538,330	03/25/2003	Forbes, Leonard	257	777	03/23/2000
JTR	US-6,559,491	05/06/2003	Forbes, Leonard , et al.	257	296	02/09/2001
JTR	US-6,566,682	05/20/2003	Forbes, Leonard	257	51	02/09/2001
JTR	US-6,582,512	06/24/2003	Geusic, Joseph E., et al.	117	3	05/22/2001
JTR	US-6,593,625	07/15/2003	Christiansen, Silke H., et al.	257	347	04/03/2002
JTR	US-6,597,203	07/22/2003	Forbes, Leonard	326	98	03/14/2001
JTR	US-6,630,713	10/07/2003	Geusic, Joseph	257	347	02/25/1999
JTR	US-6,649,476	11/18/2003	Forbes, Leonard	438	268	02/15/2001

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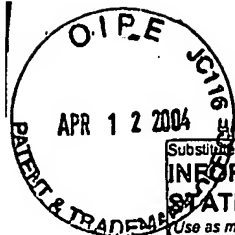
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
JTR	EP-434984	09/03/1991	Lindberg, Keith J., et al.	H01L	21/322	
JTR	WO-WO02097982	12/05/2002	Pavio, Anthony M., et al.	H03 G	3/10	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JTR		"Cornell Demonstrates a Universal Substrate", <u>Compound Semiconductor</u> , 3(2), (March/April 1997), 27-29	
JTR		ABE, T., "Silicon Wafer-Bonding Process Technology for SOI Structures", <u>Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials</u> , (1990), 853-856	
JR		AUBERTON-HERVE, A J., "SOI: Materials to Systems", <u>International Electron Devices Meeting. Technical Digest</u> , (1996), 3-10	
JTR		AUTUMN, KELLAR, et al., "Adhesive force of a single gecko foot-hair", <u>Nature</u> , 405(6787), (June 2000), 681-685	
JTR		AUTUMN, KELLAR, et al., "Evidence for van der Waals adhesion in gecko setae.", <u>Proceedings of the National Academy of Science U S A.</u> ; 99(19), (September 17, 2002), 12252-6	
JTR		BAGINSKI, T. A., "Back-side germanium ion implantation gettering of silicon", <u>Journal of the Electrochemical Society</u> , 135(7), Dept of Electrical Engineering, Auburn Univ, AL, (July 1988), 1842-3	
JTR		BELFORD, RONA E., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", <u>IEEE Device Research Conference</u> , (2002), 41-42	
JTR		BERTI, M., "Composition and Structure of Si-Ge Layers Produced by Ion Implantation and Laser Melting", <u>Journal of Materials Research</u> , 6(10), (October 1991), 2120-2126	
JTR		BERTI, M., "Laser Induced Epitaxial Regrowth of Si _{1-x} Ge _x /Si Layers Produced by Ge Ion Implantation", <u>Applied Surface Science</u> , 43, (1989), 158-164	
JTR		BIALAS, F., et al., "Intrinsic Gettering of 300 mm CZ Wafers", <u>Microelectronic Engineering</u> , 56(1-2), (May 2001), 157-63	
JTR		BIEVER, CELESTE, "Secret of 'strained silicon' revealed: behind closed doors, Intel has perfected a novel way to improve chip performance.", <u>New Scientist</u> , 180(i2426-2428), (December 20, 2003), 27	
JTR		BINNS, M. J., et al., "The Realization of Uniform and Reliable Intrinsic Gettering in 200mm P- & P/P Wafers for a Low Thermal Budget 0.18 mu m Advanced CMOS Logic Process", <u>Diffusion and Defect Data Pt.B: Solid State Phenomena</u> , 82-84, (2001), 387-92	
JTR		BRONNER, G. B., et al., "Physical Modeling of Backside Gettering", <u>Impurity Diffusion and Gettering in Silicon Symposium</u> , Sponsor: Mater. Res. Soc, Nov 1984, Boston, MA, (1985), 27-30	

EXAMINER

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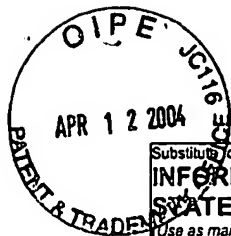
OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JAK		BROWN, CHAPPELL, "Bonding twist hints at universal substrate", <u>EETimes</u> , (1997), 2 pages	
JAK		BRUEL, M., et al., "Smart-Cut: a new silicon on insulator material technology based on hydrogen implantation and wafer bonding", <u>Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers)</u> , 36(3B), (1997), 1636-1641	
JAK		CHEN, XIANGDONG, et al., "Vertical P-MOSFETs with heterojunction between source/drain and channel", <u>IEEE Device Research Conference</u> , (2000), 25-26	
JAK		CHILTON, B T., et al., "Solid phase epitaxial regrowth of strained Si(1-x)Ge(x)/Si strained layer structures amorphized by ion implantation", <u>Applied Physics Letters</u> , 54(1), (January 2, 1989), 42-44	
JAK		CHOE, K. S., et al., "Minority-Carrier Lifetime Optimization in Silicon MOS Devices by Intrinsic Gettering", <u>Journal of Crystal Growth</u> , 218(2-4), (September 2000), 239-44	
JAK		CLARK, DON, et al., "Intel unveils tiny new transistors: Process handles circuits 1/2000th the width of a human hair", <u>The Wall Street Journal</u> , (August 13, 2002), 3 pages	
JAK		CLIFTON, P A., et al., "A process for strained silicon n-channel HMOSFETs", <u>ESSDERC'96. Proceedings of the 26th European Solid State Device Research Conference</u> , (September 1996), 519-22	
JAK		DUBBELDAY, W B., et al., "Oscillatory strain relaxation in solid phase epitaxially regrown silicon on sapphire", <u>Proceedings of the First International Workshop Lattice Mismatched Thin Films</u> , (September 13-15, 1998), 13-17	
JAK		FISCHETTI, M V., et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys", <u>Journal of Applied Physics</u> , 80(4), (August 15, 1996), 2234-2252	
JAK		FOURNEL, F., et al., "Ultra High Precision Of The Til/Twist Misorientation Angles In Silicon/Silicon Direct Wafer Bonding", <u>Abstract - Electronic Materials Conference</u> , (June 2002), 9	
JAK		GARCIA, G A., et al., "High-quality CMOS in thin (100 nm) silicon on sapphire", <u>IEEE Electron Device Letters</u> , 9(1), (January 1988), 32-34	
JAK		GODBOLE, H., et al., "An Investigation of Bulk Stacking Faults in Silicon Using Photocapacitance Transient Spectroscopy", <u>Materials Letters</u> , 8(6-7), Dept of Electr & Comput Engr, Oregon State Univ, Corvallis OR, (July 1989), 201-3	
JAK		GONG, S. S., et al., "Implantation Gettering in Silicon", <u>Solid-State Electronics</u> , 30(2), (February 1987), 209-11	
JAK		GRAF, D., et al., "300 mm epi pp- wafer: is there sufficient gettering?", <u>High Purity Silicon VI. Proceedings of the Sixth International Symposium (Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol.4218)</u> , (2000), 319-30	

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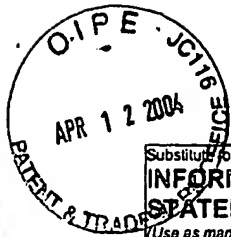
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JTR		HADDAD, H. , et al., "Carbon Doping Effects on Hot Electron Trapping", <u>28th Annual Proceedings, Reliability Physics 1990</u> , (March 1990),288-9	
JTR		HADDAD, H. , et al., "Electrical Activity of Bulk Stacking Faults in Silicon", <u>Materials Letters</u> , 7(3), Hewlett-Packard Northwest Integrated Circuits Div, Corvallis OR,(September 1988),99-101	
JTR		HARENDT, CHRISTINE , "Silicon on Insulator Material by Wafer Bonding", <u>Journal of Electronic Materials</u> , 20(3), (March 1991),267-77	
JTR		IYER, S S., "Separation by Plasma Implantation of Oxygen (SPIMOX) operational phase space", <u>IEEE trans. on Plasma Science</u> , 25, (1997),1128-1135	
JTR		KALAVADE, PRANAV , et al., "A novel sub-10 nm transistor", <u>58th DRC. Device Research Conference. Conference Digest</u> , (June 19-21, 2000),71-72	
JTR		KANG, J. S., et al., "Gettering in Silicon", <u>Journal of Applied Physics</u> , 65(8), Center for Solid State Electron Res., Arizona State Univ., Tempe, AZ,(April 15, 1989),2974-85	
JTR		KOSTRZEWA, M , et al., "Testing the Feasibility of strain relaxed InAsP and InGaAs compliant substrates", <u>EMC 2003 International Conference Indium Phosphide and Related Materials. Conference Proceedings</u> , Other authors: G. Grenet et al,(6/2003),8-9	
JTR		KUNG, C. Y., et al., "The effect of carbon on oxygen precipitation in high carbon CZ silicon crystals", <u>Materials Research Bulletin</u> , 18(12), Silicon Materials Div., Fairchild Camera & Instrument Corp, Healdsburg, CA,(December 1983),1437-41	
JTR		LASKY, J. B., "Wafer Bonding for Silicon-on-Insulator Technologies", <u>Applied Physics Letters</u> , 48(1), (January 6, 1986),78-80	
JTR		LI, Y. X., et al., "New intrinsic gettering process in Czochralski-silicon wafer", <u>6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings</u> , 1(1), (2001),277-9	
JTR		LOO, Y L., et al., "Contact Printing With Nanometer Resolution", <u>Device Research Conference</u> , (June 2002),149-150	
JTR		LU, D. , "Bonding Silicon Wafers by Use of Electrostatic Fields Followed by Rapid Thermal Heating", <u>Materials Letters</u> , 4(11), (October 1986),461-464	
JTR		MIZUNO, T , et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS Electron/Hole Mobility Enhancement", <u>2000 Symposium on VLSI Technology. Digest of Technical Papers</u> , (2000),210-211	
JTR		MORAN, PETER , "Strain Relaxation in Wafer-Bonded SiGe/Si Heterostructures Due to Viscous Flow of an Underlying Borosilicate Glass", <u>Electronic Materials Conference, Santa Barbara, June 2002, Abstract</u> , (June 2002),Pgs. 8-9	
JTR		MUMOLA, P. B., et al., "Recent advances in thinning of bonded SOI wafers by plasma assisted chemical etching", <u>Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications</u> , (1995),28-32	

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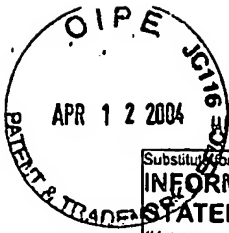
OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

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JTR		NAYAK, D.K., "High performance GeSi quantum-well PMOS on SIMOX", <u>International Electron Devices Meeting 1992. Technical Digest</u> , (1992),777-80	
JTR		O'NEILL, A G., et al., "High speed deep sub-micron MOSFET using high mobility strained silicon channel", <u>ESSDERC '95. Proceedings of the 25th European Solid State Device Research Conference</u> , (September 1995),109-12	
JTR		OMI, HIROO, et al., "Semiconductor Surface with Strain Control", http://www.brl.ntt.co.jp/J/kouhou/katsudou/report00/E/report04_e.html , (January 2000)	
JTR		OR, B S., et al., "Annealing effects of carbon in n-channel LDD MOSFETs", <u>IEEE Electron Device Letters</u> , 12(11), Dept of Electrical & Computing Engr, Oregon State Univ, Corvallis OR, (November 1991),596-8	
JTR		OUYANG, Q, et al., "Bandgap Engineering in Deep Submicron Vertical pMOSFETs", <u>IEEE 58th DRC. Device Research Conference. Conference Digest</u> , (2000),27-28	
JTR		PAINE, D. C., "The Growth of Strained Si _{1-x} Ge _x Alloys on (100) Silicon Using Solid Phase Epitaxy", <u>Journal of Materials Research</u> , 5(5), (May 1990),1023-1031	
JTR		PEOPLE, R., "Calculation of critical layer thickness versus lattice mismatch for GeSi _{1-x} /Si strained-layer heterostructures", <u>Applied Physics Letters</u> , 47(3), (August 1, 1985),322-4	
JTR		RIM, KERN, et al., "Fabrication and analysis of deep submicron strained-Si n-MOSFETs", <u>IEEE Transactions on Electron Devices</u> , 47(7), (July 2000),1406-1415	
JTR		RIM, KERN, et al., "Strained Si NMOSFETs for High Performance CMOS Technology", <u>2001 Symposium on VLSI Technology. Digest of Technical Papers</u> , (2001),59-60	
JTR		RIM, KERN, et al., "Transconductance enhancement in deep submicron strained Si n-MOSFETs", <u>International Electron Devices Meeting 1998. Technical Digest</u> , (1998),707-710	
JTR		RUBIN, L, et al., "Effective gettering of oxygen by high dose, high energy boron buried layers", <u>1998 International Conference on Ion Implantation Technology. Proceedings</u> , 2(2), (1998),1010-13	
JTR		SATO, T, "Trench transformation technology using hydrogen annealing for realizing highly reliable device structure with thin dielectric films", <u>1998 Symposium on VLSI Technology Digest of Technical Papers</u> , (1998),206-7	
JTR		SUGIYAMA, N, et al., "Formation of strained-silicon layer on thin relaxed-SiGe/SiO ₂ /sub 2//Si structure using SIMOX technology", <u>Thin Solid Films</u> , 369(1-2), (July 2000),199-202	
JTR		TAKAGI, SHIN-ICHI, "Strained-Si- and SiGe-On-Insulator (Strained-SOI and SGOI) MOSFETs for High Performance/Low Power CMOS Application", <u>IEEE Device Research Conference, 2002. 60th DRC. Conference Digest</u> , (2002),37-40	

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JTR		TAN, T. Y., et al., "Intrinsic gettering by oxide precipitate induced dislocations in Czochralski Si", <u>Applied Physics Letters</u> , 30(4), IBM System Products Div., Essex Junction, VT, (February 15, 1977), 175-6	
JTR		VERDONCKT-VANDEBROEK, SOPHIE, et al., "SiGe-Channel Heterojunction p-MOSFET's", <u>IEEE Transactions on Electron Devices</u> , 41(1), (January 1994), 90-101	
JTR		WELSER, J, et al., "Strain dependence of the performance enhancement in strained-Si n-MOSFETs", <u>IEEE International Electron Devices Meeting 1994, Technical Digest</u> , (December 11-14, 1994), 373-376	
JTR		WHITWER, F. D., et al., "DLTS characterization of precipitation induced microdefects", <u>Materials Issues in Silicon Integrated Circuit Processing Symposium</u> , (April 1986), 53-57	
JTR		WIJARANAKULA, W., et al., "Effect of Pre- and Postepitaxial Deposition Annealing on Oxygen Precipitation in Silicon", <u>Journal of Materials Research</u> , 1(5), Dept of Electr & Comput Eng, Oregon State Univ, Corvallis, OR, (September-October 1986), 698-704	
JTR		WIJARANAKULA, W., et al., "Effect of preanneal heat treatment on oxygen precipitation in epitaxial silicon", <u>Materials Issues in Silicon Integrated Circuit Processing Symposium</u> , (April 1986), 139-44	
JTR		WIJARANAKULA, W., et al., "Internal Gettering Heat Treatments and Oxygen Precipitation in Epitaxial Silicon Wafers", <u>Journal of Materials Research</u> , 1(5), Dept of Electr & Comput. Eng, Oregon State Univ., Corvallis, OR, (September-October 1986), 693-7	
JTR		WIJARANAKULA, W., et al., "Oxygen precipitation in p/p+(100) epitaxial silicon material", <u>Journal of the Electrochemical Society</u> , 134(9), SEH America, Inc., Mater. Characterization Lab., Vancouver, WA, (September 1987), 2310-16	
JTR		XUAN, PEIQI, et al., "60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOSFETs", <u>IEEE Device Research Conference, Conference Digest. 58th DRC</u> , (June 19-21, 2000), 67-68	
JTR		YANG, D., et al., "Intrinsic Gettering in Nitrogen Doped Czochralski Crystal Silicon", <u>High Purity Silicon VI. Proceedings of the Sixth International Symposium (Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol. 4218)</u> , (2000), 357-61	
JTR		YANG, DEREN, et al., "Nitrogen in Czochralski Silicon", <u>2001 6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings</u> , 1(1), (2001), 255-60	

EXAMINER

DATE CONSIDERED

8/31/04



Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	10/052952
	Filing Date	January 17, 2002
	First Named Inventor	Forbes, Leonard
	Group Art Unit	2874
	Examiner Name	Rahll, Jerry
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
Jm3		YIN, HAIZHOU, "High Ge-Content Relaxed Si1-xGe1-x Layers by Relaxation on Complaint Substrate with Controlled Oxidation", <u>Electronic Materials Conference, Santa Barbara, June 2002, (June 2002),8</u>	
JTR		ZHU, Z H., et al., "Wafer bonding and its application on compliant universal (CU) substrates", <u>Conference Proceedings, 10th Annual Meeting IEEE Lasers and Electro-Optics Society, (November 10-13, 1996),31</u>	
JTR		ZHU, Z H., et al., "Wafer bonding technology and its applications in optoelectronic devices and materials", <u>IEEE Journal of Selected Topics in Quantum Electronics, (June 1997),927 - 936</u>	

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DATE CONSIDERED

8/13/04